Spring 5-8-2015

Systematic Characterization Measurements of GST Nano Line Cells

Lindsay Sullivan
lindsay.sullivan@uconn.edu

Systematic Characterization Measurements of GST Nano Line Cells

Lindsay Sullivan

University of Connecticut

Department of Electrical and Computer Engineering

Honors Thesis

May 2015

Honors Research Advisors: Ali Gokirmak & Helena Silva

Abstract

$Ge_2Sb_2Te_5$ nano line cells cycled most successfully between the amorphous and crystalline states when a continuous SET-RESET pulse was applied with a square 20 ns amorphization pulse and a 3.5 μs crystallization pulse. The crystalline pulse had a 1 μs ramped incline and a 2 μs ramped decline. The resistance window between the SET and RESET states drastically declined if the amplitude of the SET-RESET waveform was not increased. In resistance drift measurements, the device cycled 10 times had a higher stabilized crystalline resistance than the device only cycled once. These results suggest that cycling a device multiple times disturbs the wires so that the stable crystalline resistance is higher than that of the devices which are only set once (or not cycled at all). An RC time delay was observed when an AC signal was applied to amorphized wires with a 1 MΩ termination resistance. It is hypothesized that two parasitic Schottky diodes are forming between the contact metal and the semiconductor material and causing the unusual charging and discharging. A new model of the experimental set-up has been created to account for this phenomenon.

Acknowledgements

First, I would like to thank my research advisors Ali Gokirmak and Helena Silva. They both have so much the kindness and patience for their students. I would also like to thank the associate head of the Electrical and Computer Engineering (ECE) department, John Chandy, for always having an open door policy for the panicking seniors. I would like to say a big thank you to Faruk Dirisaglik, Gokhan Bakan, Kadir Cil, Zoila Jurado, and the rest of the Nano electronics lab for being so helpful with my research and stepping in as an impromptu family while I am so far away from home. Finally, thank you to the staff of the ECE department for being so supportive of your students and always doing your best to help us succeed.

Contents

Introduction

As computer processor speed increases and size decreases, memories such as dynamic random access memory (DRAM) and static random access memory (SRAM) are falling short of expectations in size and cost.[1] The discovery of flash memory as a solid state memory solution bridges the gap between hard-drives and DRAM, and for this reason, researchers have turned to non-volatile memory in hopes of finding a solution to DRAM's current constraints. Phase change memory (PCM) has emerged and developed into a strong contender as a solution to the next generation of memory.[1]

Due to of DRAM's volatile nature, and the growing size of the memory systems, it has already exceeded competitive power cost and consumption limits. Flash memory, like PCM, is a non-volatile memory, meaning it can retain information without being powered. But, while Flash memory can only endure 10^4-10^5 read/write cycles, PCMs are capable of enduring closer to 10^8 cycles.[2] DRAM has an almost infinite cycle capability, but it is usually much larger than both the PCM and flash memory solutions due to the size of the capacitor needed to hold a detectable charge. Although Flash memory is the most dense of the three memories, it has the slowest access latency (about 200x slower than DRAM), while PCMs are only 4x slower than DRAM and make up for it by being 4x as dense.[2]

Due to its comparable speed, life-time, and density, the study of PCMs as a viable bridge between flash memory and DRAM has rapidly increased over the past 20 years. PCM applies the characteristic transition of chalcogenides between a highly resistive (amorphous) and a highly

conductive (crystalline) state to simulate a devices ON and OFF states respectively. The electrical resistances of these states determine the logic state of the device (1 or 0) and can be toggled with the use of electrical pulses. Generally, a memory device requires two orders of magnitude between the ON and OFF state to successfully operate, and PCM devices are capable of consistently reaching a resistivity contrast of ~5 orders of magnitude between the crystalline and amorphous states. Semiconductor alloys in the GeTe-Sb2Te3 pseudobinary line have the capability of enduring the most SET-RESET cycles and at the fastest rate. The most commonly researched PCM composition is $Ge_2Sb_2Te_5$ (GST).[1]

To Set a device, the semiconductor material needs to be melted and then quenched almost instantaneously to catalyze an atomic structural change. This is done by sending a very short electrical pulse (10-20 ns) through the wire. A longer pulse and/or higher pulse amplitude creates a larger amorphous region and consequentially a higher resistance. It is best to keep the amorphous region small so that recrystallizing the device is possible. The crystallizing electrical pulses generally have a lower amplitude and a much longer duration than the pulses used to amorphize the device. Re-crystallization (RESET) is achieved by slowly heating up the wire to induce growth of crystalline nuclei. As the temperature of the device increases, an increased rate of nucleation occurs, and the grains continue to grow until their grain boundaries touch. Once they have grown large enough to reach a stable state, the physical change of electric properties can be observed.[5]

Many different characteristics of GST have been recently studied, including resistance drift due to structure relaxation, recrystallization speed at various temperatures, and dimension and shape of the devices. For this experiment, $Ge_2Sb_2Te_5$ (GST) nano line cells are characterized while undergoing different set-reset waveforms. The aim of these measurements is to design a

waveform that better optimize the cycling process. A new model of the current experimentation set-up is simulated to encompass a new RC charging and discharging that was observed while using a 1 MΩ termination resistance. This new model helps gather a better understanding of results taken when measuring with this experimental set-up.

Experiment Set-up

$Ge_2Sb_2Te_5$ (GST) is the composition used in the nano line cells in this experiment. The devices were fabricated by Faruk Dirisaglik, Adam Cywar, Kadir Dirisaglik, and Mustafa at the IBM T.J. Watson Research Center.

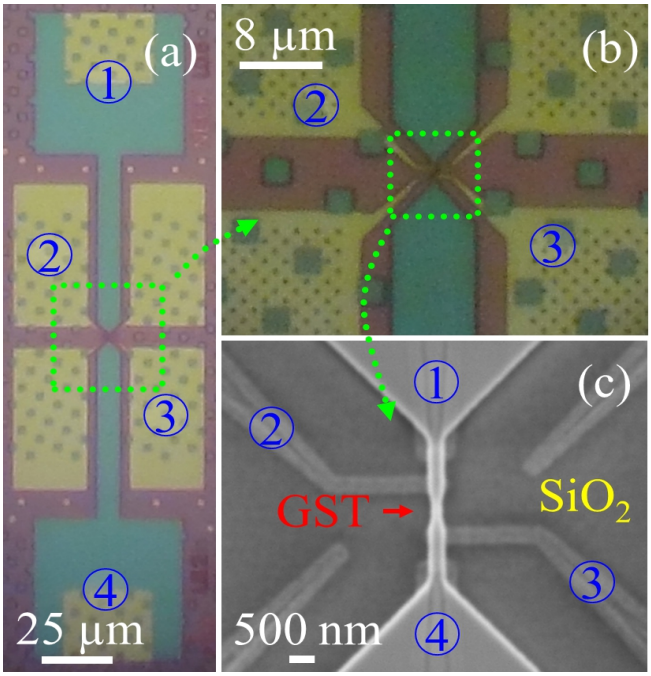


Figure 1: Optical microscope (a,b) and SEM (c) images (taken by Faruk Dirisaglik) of the four contact devices used in the measurements.

Length and width dimensions of the devices in this paper are reported in nanometers. All measurements were performed at room temperature (300K) unless specified otherwise.

The wires were all measured using a cryogenic probe station (Figure 1). Voltage waveforms are sent from the computer to a function generator and into the device using two probes from the probe station. A digital phosphor oscilloscope is also attached to these two probes so that the response of the wire to the waveform can be captured and analyzed. A parameter analyzer is connected to another set of probes in the station so that the resistance of the devices can be taken by sending and analyzing an I-V sweep.

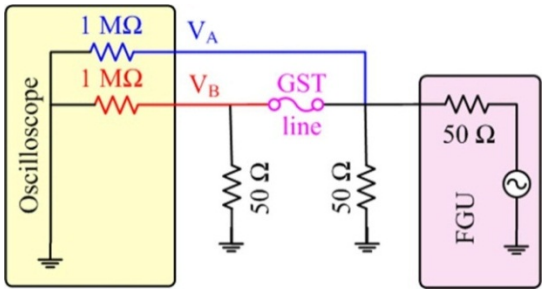


Figure 2: Circuit schematic of the probe station used for measurements.

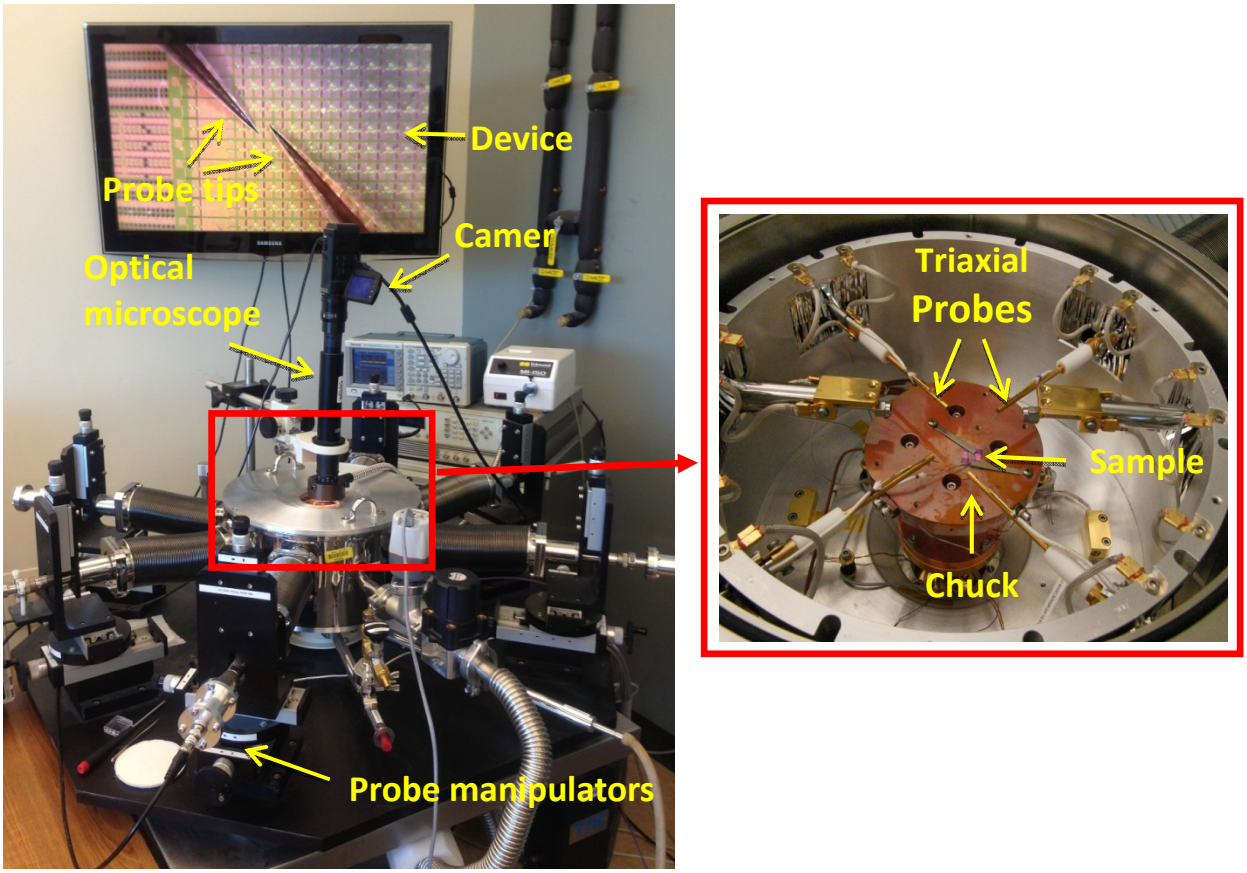


Figure 3: Experimental set-up used to measure the nano-devices. The image on the right shows a closer look at the inside of the station where the device chip is placed.

Cycling: Set and Reset Waveforms

Maximizing the cycling capabilities of phase-change devices with a uniform process is vital to making PCM a viable commercially produced memory solution. Characterizing how the material behaves during the set and reset periods is important in understanding how the devices will react during multiple cycling periods. In these measurements, the electrical pulses used to amorphize the devices were between 10-20 ns. The voltage amplitude during the pulse varied based off of

the device resistance and dimensions. The crystallization pulses used in these measurements were between 1-5 µs.

The first attempt at cycling began with using square amorphizing and crystallizing pulses. The success of each waveform was recorded as the pulse length, amplitude, slope, and offset were changed. The goal was for the waveform to be able to amorphize and then recrystallize a GST wire by using one continuous waveform. The most successful of the arbitrary waveform tested contained an AC read signal preceded by a RESET pulse and followed by a SET pulse.

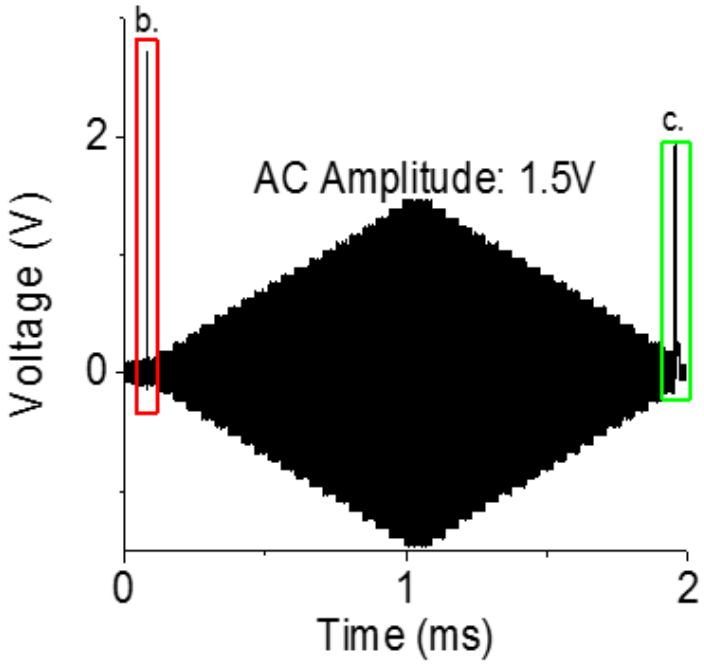


Figure 4: This reset and set AC waveform was used to cycles several devices six times, leaving the devices in a crystalline state. The waveform contains an amorphization pulse (boxed in red), an AC signal with the frequency of 1MHz and amplitude of 1.5V, and a set pulse (boxed in green). The voltage of the reset and set pulse were subject to change depending on the resistance and dimensions of the device.

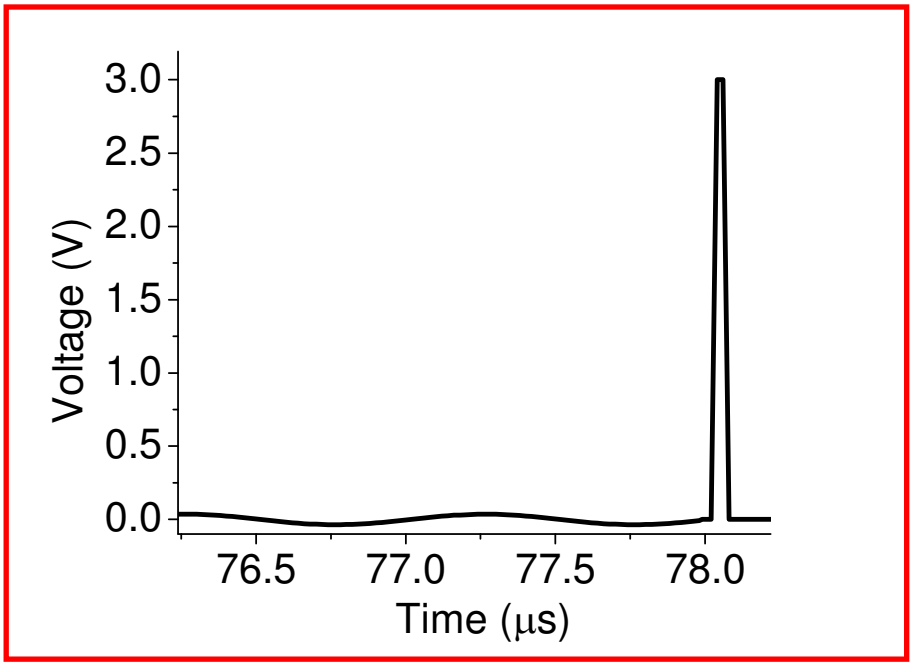


Figure 4b: An enlarged view of the amorphization pulse from the reset/set waveform using an AC signal.

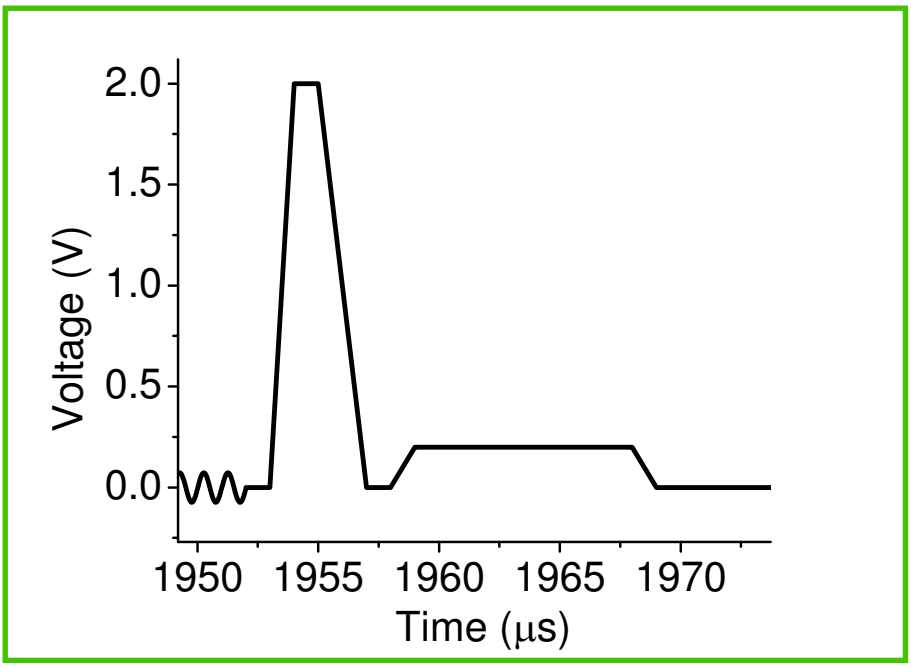


Figure 4c: An enlarged view of the crystallization pulse from the reset/set waveform using an AC signal.

The waveform in Figure 4 contains an amorphization pulse (boxed in red), an AC read signal with the frequency of 1MHz and amplitude of 1.5V, and a set pulse (boxed in green). The amorphization pulse (Figure 4b) has a 20ns rise time, flate time and fall time, for a total of 60ns.

The crystallization pulse (Figure 4c) has 1µs rise time, flate time and 2µs fall time, for a total of 4µs. The small voltage applied after the set pulse visually shows that the wire has returned to a crystalline state.

As an example, for one device, the waveform used in the first cycle contained a 2.75V pulse with the AC amplitude of 1.5V. When sending the waveform for multiple cycles, the AC portion of the signal repeatedly recrystallized the device prior to the set pulse. To account for this, the amplitude of the AC read waveform was reduced by half so that the amplitude was not high enough to disturb the device.

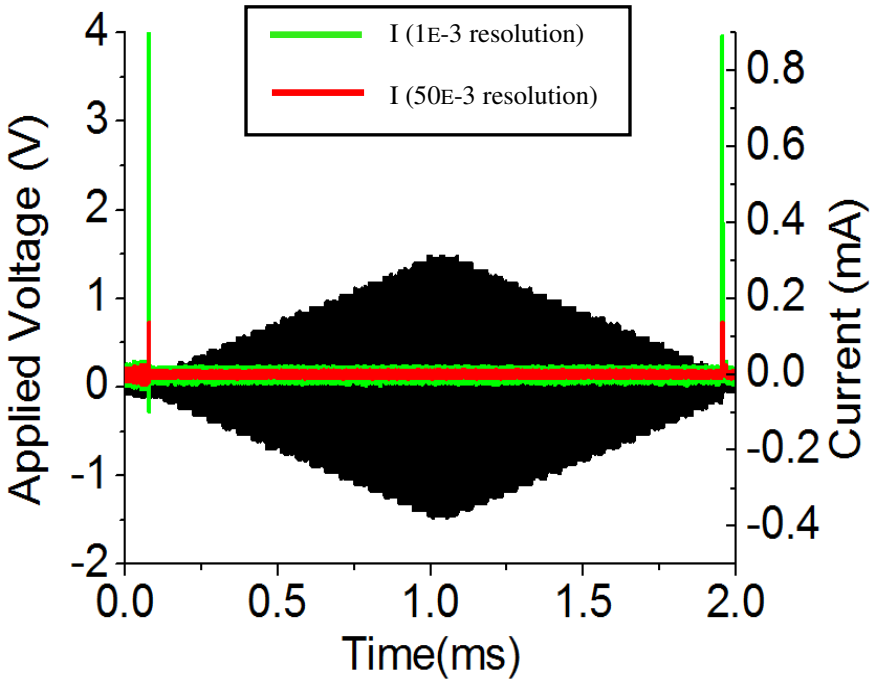


Figure 5: The first cycle of the device. Both measured currents (red and green) are the same, the data from the green line was acquired using a different channel and has a lower resolution.

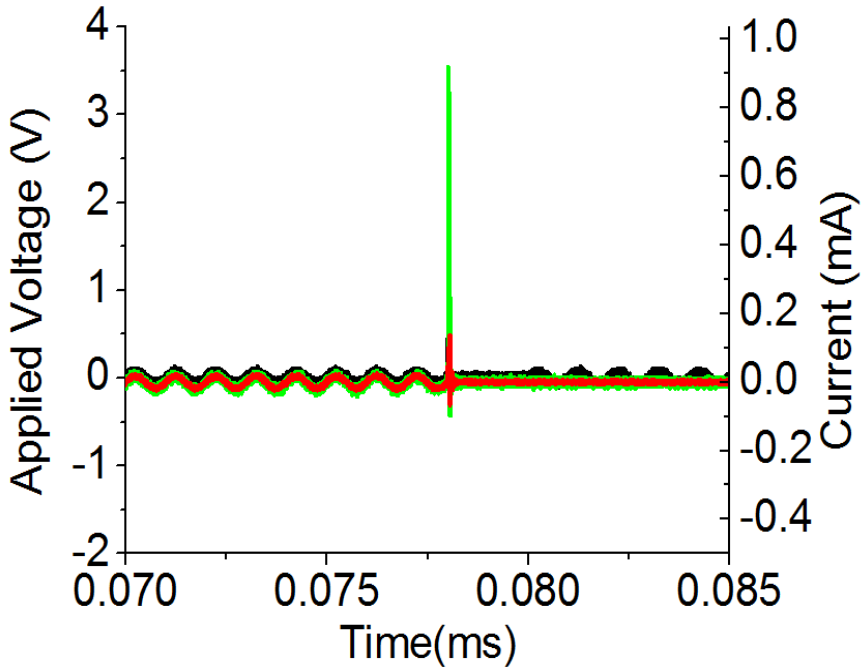


Figure 5b: An enlarged view of the amorphization pulse and measured current from the reset/set waveform using an AC signal.

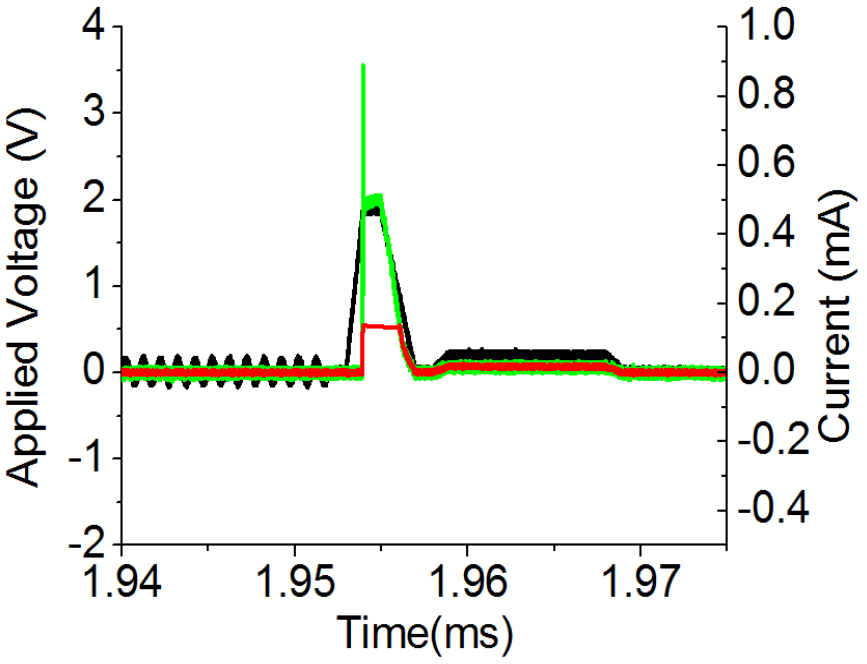


Figure 5c: An enlarged view of the crystallizing pulse and measured current from the reset/set waveform using an AC signal.

Figure 5 contains the entire cycle of a wire that was RESET and then SET. The red and green lines show the current flowing through the device with two different resolutions, and the black line is the applied voltage waveform. Figure 5b shows a closer view of the amorphization pulse. The current (red and green) follows the applied voltage before the amorphization pulse, indicating that the wire is at a low resistance value (crystalline). After the initial pulse, the current levels are very low, indicating that the wire is now very resistive or amorphous. Each run is not considered a cycle unless the wire is amorphized to a high enough resistance so that the current no longer reacts to the applied voltage. If the device did not fully amorphize with the pulse, the initial amorphizing pulse was increased and the waveform was resent. In Figure 5c, the SET pulse is shown on a closer scale. Before the pulse, the current level is very low (noise level is significantly larger than the AC signal)- indicating that the wire is still in the amorhous state. After the SET pulse, the current reacts to the small square wavefore- indicating that it is now crystalline once again. The sudden increase in current during the pulse indicates the point of melting or crystallization. The amorphous resistance after reset pulse, resistance at set pulse, and resistance after set pulse can be found by analyzing these melting points.

The length of amorphized wire for the devices were calculated using current/voltage plots similar to Figure 5c. To do this, the breakdown field of GST (assumed to be 0.0056 V/nm) and the threshold voltage (the voltage that correlates to a jump in current) were used as shown in the formula below.

$$\frac{V_{Threshold}}{E_{Breakdown}} = L_{Amorphized}$$

The following equation is an example of the calculation of the amount amorphized during the first cycle for the device with dimensions 50 nm (length) x 62 nm (width). The amount amorphized for each cycle was calculated and can be seen in Table 1.

$$\frac{1.83V}{.0056\,{}^{V}/_{nm}} = 32.68\,nm$$

Cycle #	Initial Crystalline Resistance (Ω)	Breakdown (V)	Amount Amorphized (nm)
1	8.00E+03	1.83	32.68
2	1.10E+04	1.63	29.11
3	1.63E+04	1.87	33.39
4	1.66E+04	1.91	34.11
5	6.98E+03	1.47	26.25
6	5.43E+03	1.23	21.96

Table 1: The length of the amorphous region during each cycle of a GST wire with size L50W62 of die 64215-1 50nm GST on Oxide. The device was left at crystalline state after the six cycled were completed..

The amorphous resistance was also calculated using this Reset/Set waveform. Each resistance was then compared to the amount amorphized to formulate a relationship between the two. From the calculations, no strong correlations are seen between the amount amorphized or the amorphous resistance and the final crystalline resistance after the cycle. However, with the exception of one outlier, there is a correlation between the amount amorphized and the amorphous resistance (See Figure 6). As the amorphous resistance increases, so does the amount of amorphized wire.

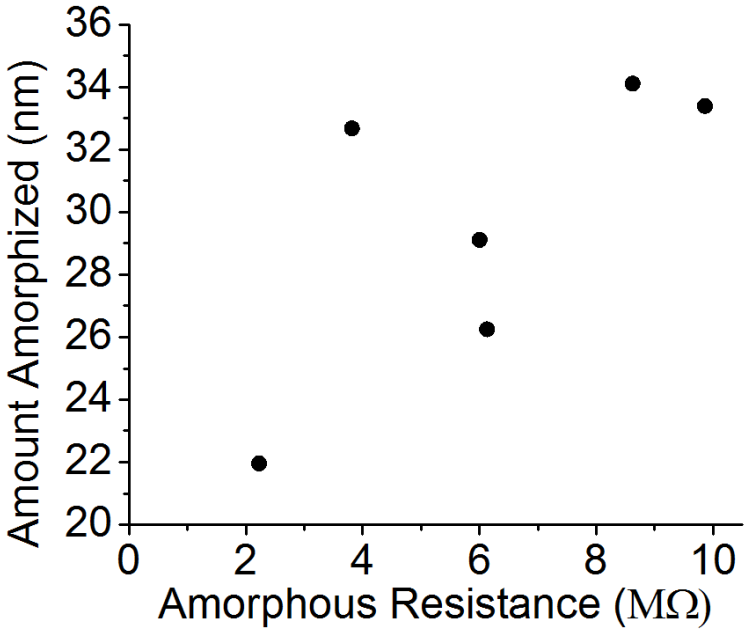


Figure 6: A scatter plot showing the positive correlation between the amorphous resistance and the expected amount amorphized (in nm).

Amount Amorphized (nm)	Amorphous Resistance (Ω)	Resistance at Set Pulse (Ω)	Final Crystalline Resistance (Ω)
32.68	3.818E+06 ± 1.878E+05	3.800E+03	1.10E+04
29.11	6.003E+06 ± 4.702E+05	3.753E+03	1.63E+04
33.39	9.859E+06 ± 1.548E+06	3.697E+03	1.66E+04
34.11	8.622E+06 ± 1.001E+06	3.679E+03	6.98E+03
26.25	6.130E+06 ± 4.852E+05	3.667E+03	5.43E+03
21.96	2.228E+06 ± 1.039E+05	3.665E+03	1.54E+03

Table 2: The amount amorphized during each reset pulse on wire L50W62 and the resistances at different stages during the cycling process. The device was left at crystalline state after the six cycled were completed

An important characteristic of GST material is the window between the resistive states as a device is cycled. It is important to keep this window larger than 2 orders of magnitude apart to

guarantee successful memory retention. The window between the amorphous and crystalline resistance for a device can be seen in Figure 7. This window consistently held a 3-4 magnitude gap between the amorphous and crystalline states.

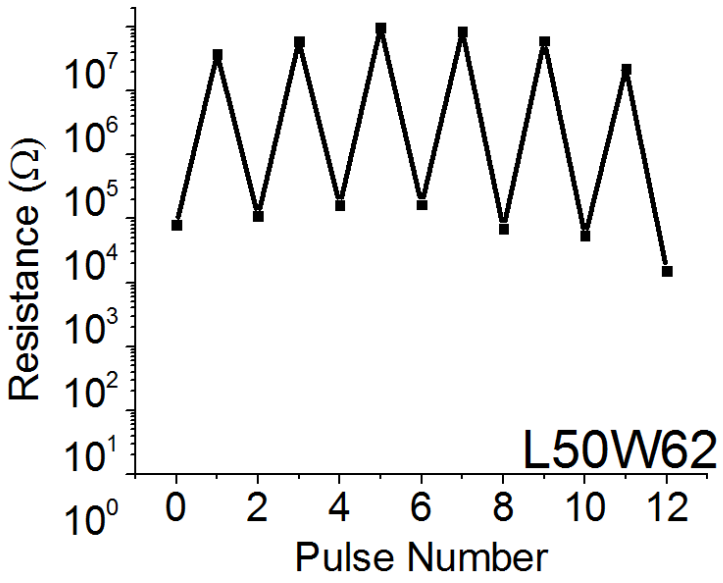


Figure 7: The cyclic processed accomplished by cycling the device L50W62 six times using the continuous SET/RESET waveform. The cycling window is demonstarated

After completing the first round of cycling measurements, new cycles were performed using the waveform from J. L. M. Oosthoek's paper, "Evolution of cell resistance, threshold voltage and crystallization temperature during cycling of line-cell phase-change random access memory."

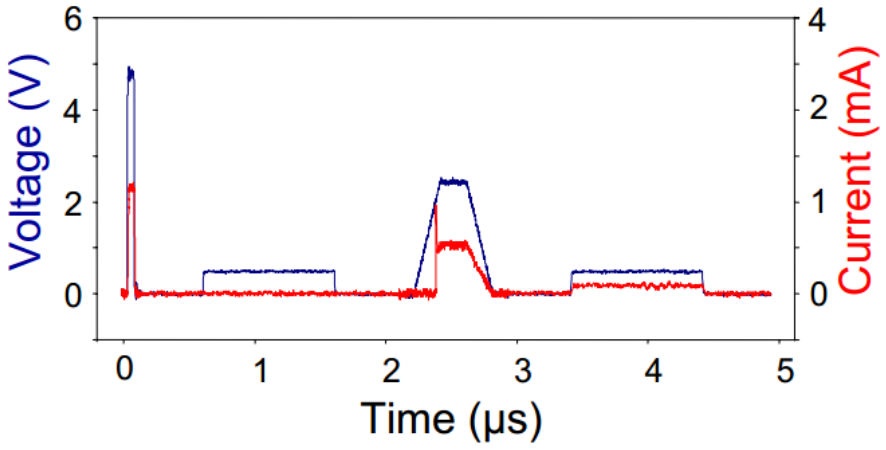


Figure 8: J. L. M. Oosthoek's waveform in which he used to cycle devices at 400K.

This waveform was chosen as the template for a new set of cycling due to the numerous variables that could easily be changed and its published success. During experimentation, the maximum voltage for both the set and reset pulses were varied, along with the slope of the crystallizing pulse both during the rising and falling times of the maximum voltage. It was also necessary to change the duration of the crystallization pulse to recycle the devices in this measurement. After observing the effect of changing these specified waveform variables, the waveform in Figure 9 successfully cycled the most devices during testing.

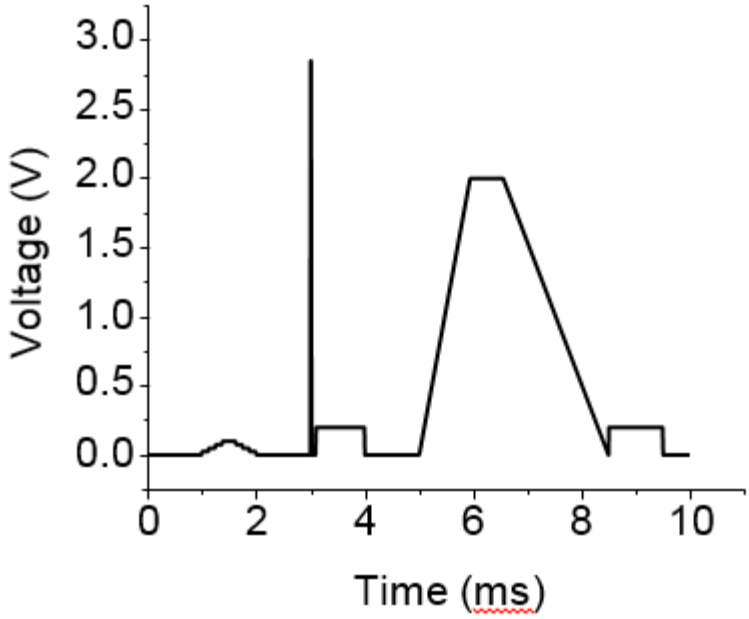


Figure 9: An example of a waveform with both the SET and RESET pulses, inspired by J. L. M. Oosthoek's waveform.

The waveform begins with a small DC step read to ensure that the wire is there and that it is in a crystalline state. The reset pulse is a short 20 ns pulse that is varied depending on the initial crystalline resistance of the device. The small rectangular read pulse after the amorphization pulse is there to visually show that the wire has become amorphous. Following this is the SET pulse. The set pulse lasts 3.5 µs, with a 1 µs rise time, a 0.5 µs constant maximum voltage, and a 2 µs fall time. The long (SET) pulse is followed by another small rectangle to visually show the ending phase of the device. Figure 10 is an example of a cycled device using this waveform with both the melted and crystalline resistances calculated.

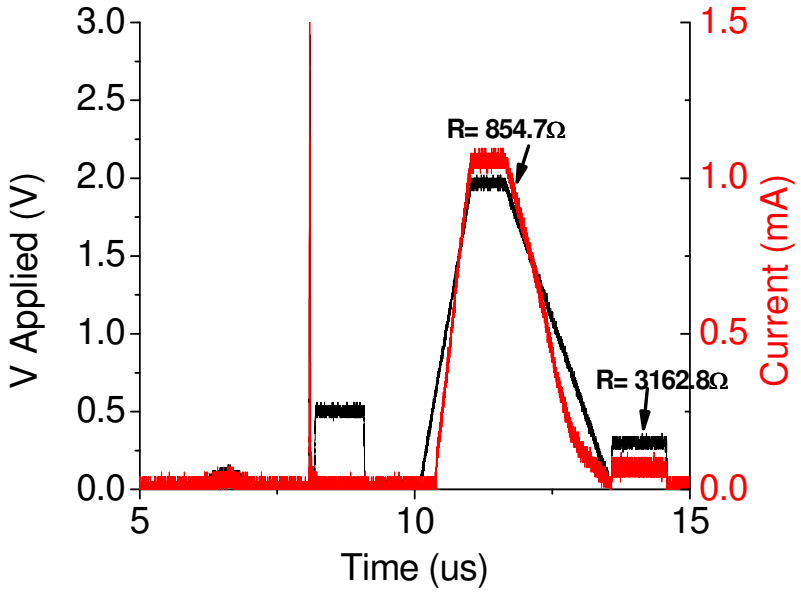


Figure 10: An example of a cycled devive. The SET/RESET waveform is in black and the measured current is in read.

The disadvantage of this waveform is the inability to measure the amorphous resistance after the reset pulse. It is still possible to calculate the resistance during the set pulse and the crystalline resistance after a complete cycle. The molten resistance of the wire was calculated to be 854.7Ω, as presented in Figure 10. These results match another device, which had a similar resistance at that state (850Ω).

To save time, ten of these waveforms were combined into one continuous signal to see how many cycles could be successfully completed in one run.

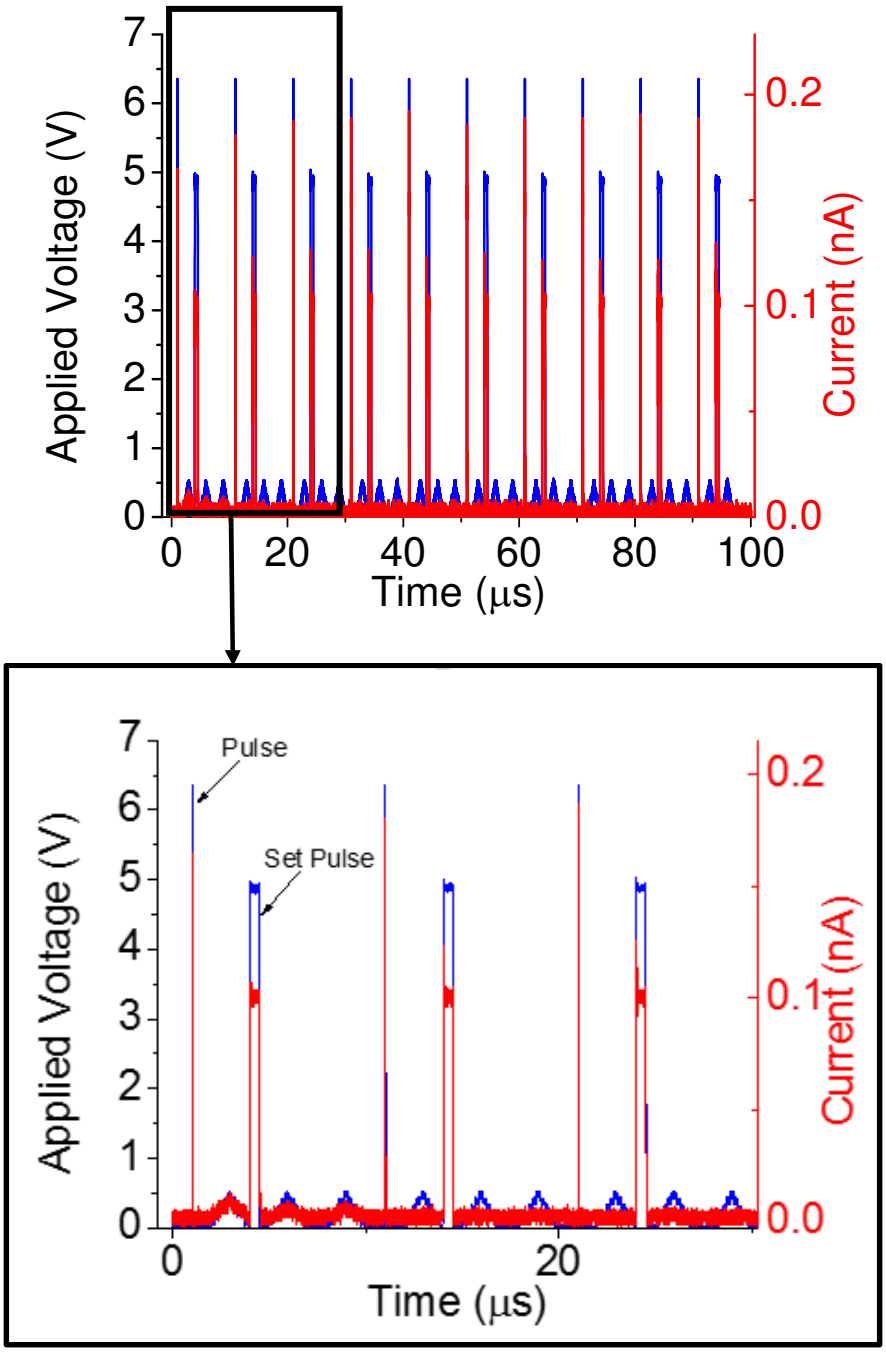


Figure 11: An image of the 10 combined waveforms from the function generator (blue) and the current measured through the wire (red).

Figure 11b: An enlarged view of the first three pulses. This device only cycled during the first pulse and remained amorphous the rest of the signal.

Some devices were able to undergo 19 cycles with this method by sending the signal twice. As the function generator sent each pulse, the resulting crystalline resistance would increase until it

reached around 200 kΩ. After this point, the device was amorphized in the same manner but was not able to be set again with this waveform due to the high resistance value. The device could only be SET again with individual (and higher voltage) pulses once this happened.

The previous measurements were done using a 1 kΩ load resistor that was already inherently part of the probe. This load resistor was too low and made it easy to break the wires or amorphize too large of a portion of the wire. To correct this, a 3 kΩ resistor was added in series to a 1 kΩ probe to create a 4 kΩ load resistor (Shown in Figure 12).

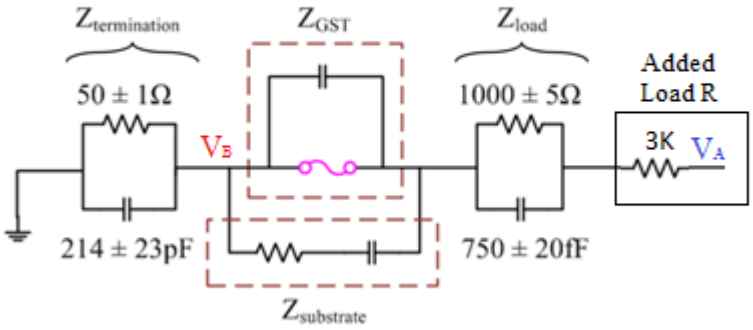


Figure 12: Circuit schematic including parasitic elements and added load resistor.

With a larger load, less current was passed across the device during its low resistive state, and it became easier to amorphize smaller portions of the wire without breaking it. Figure 13 shows an example of a cycle with this altered set-up.

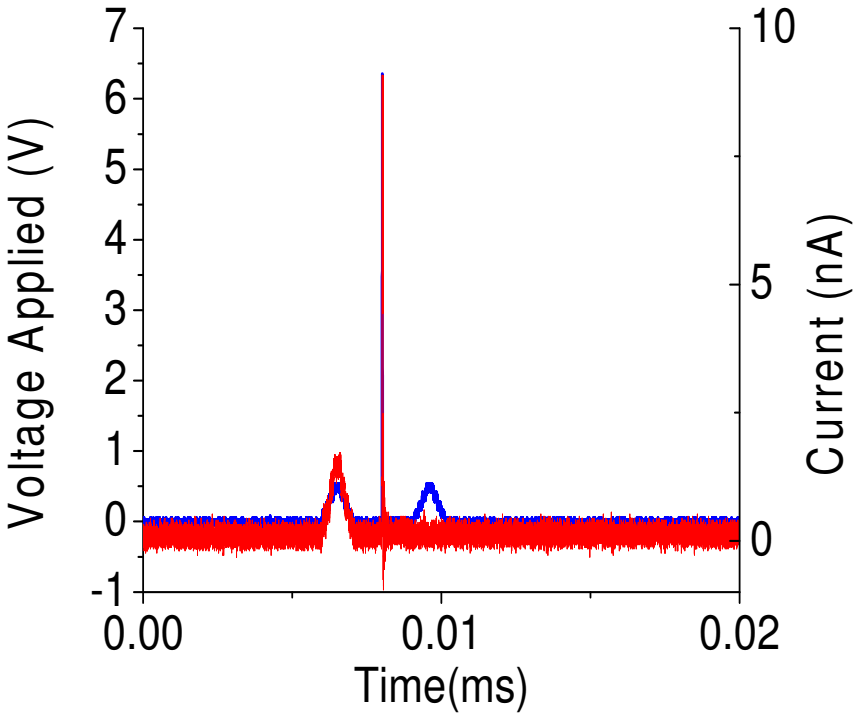


Figure 13: An example of the RESET pulse (blue) with measured current through the device (red).

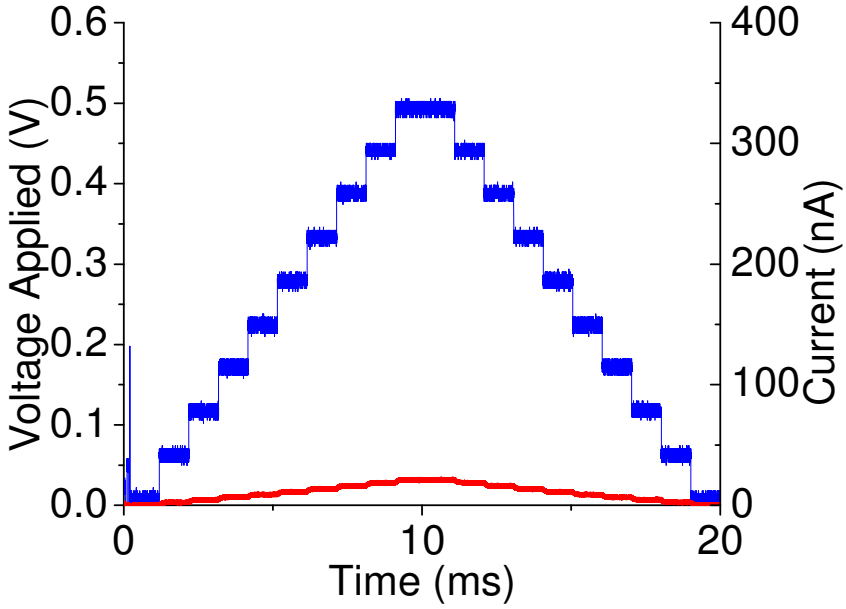


Figure 13b: The DC step waveform sent after amorphization (blue) and the current through the wire (red).

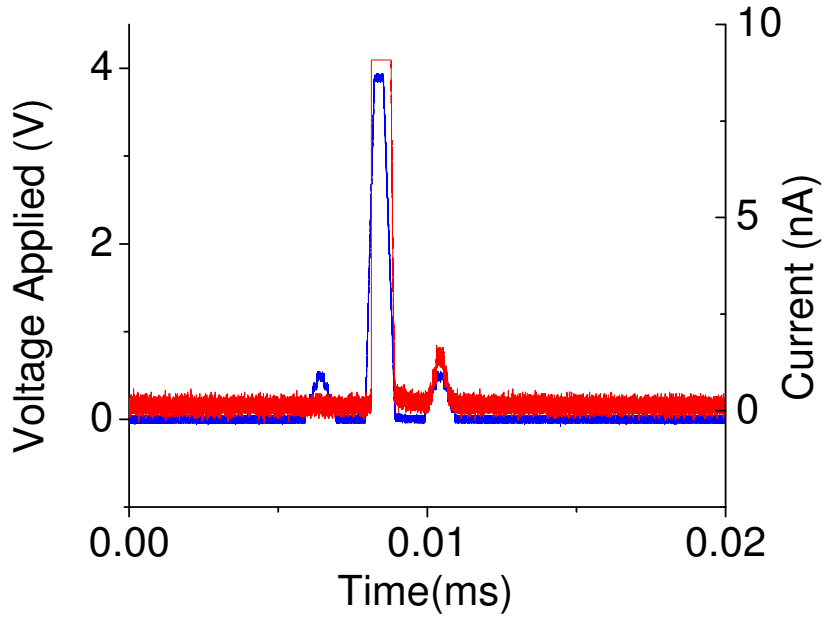


Figure 13c: An example of the SET puslse (blue) with the measured current through the device (red).

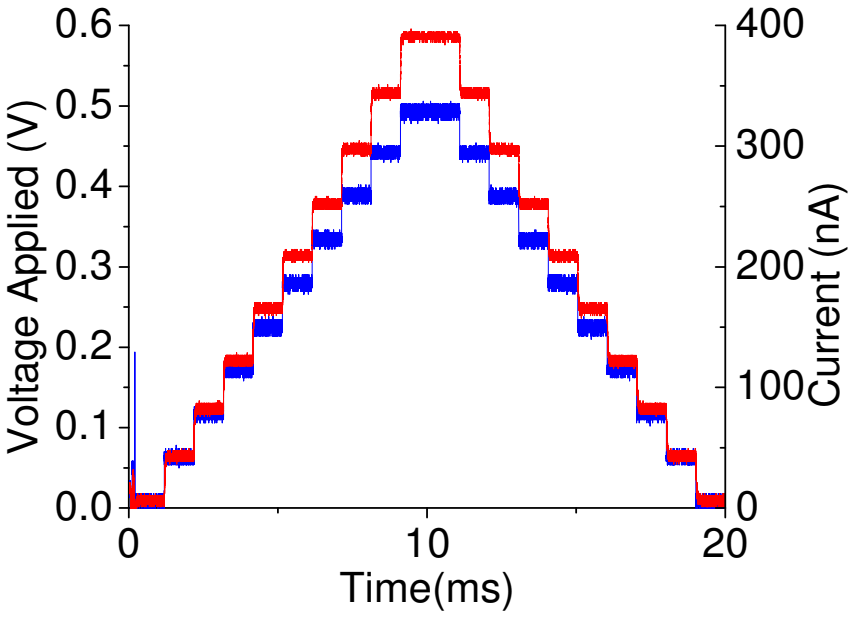


Figure 13d: The DC step waveform sent after crystallization to measure the resistance through the wire.

One device was cycled 34 times using this new set-up, and the wire was left in crystalline state. The DC steps shown in Figures 13b and 13d were sent after each pulse so that the resistance of the wire could be calculated without changing the probes. The process was slow because the

same signal could not consistently be sent for each cycle. The longest period of cycles that could be made with the same waveform was 10 cycles, but even then, the Set-Reset window decreased with each cycle. In most cases, the SET pulse needed to be sent multiple times or at different voltages to crystallize the device. Even with the fine control over the voltage pulse sent to the device, the overall trend of the window between the amorphous and crystalline resistances began to decrease.

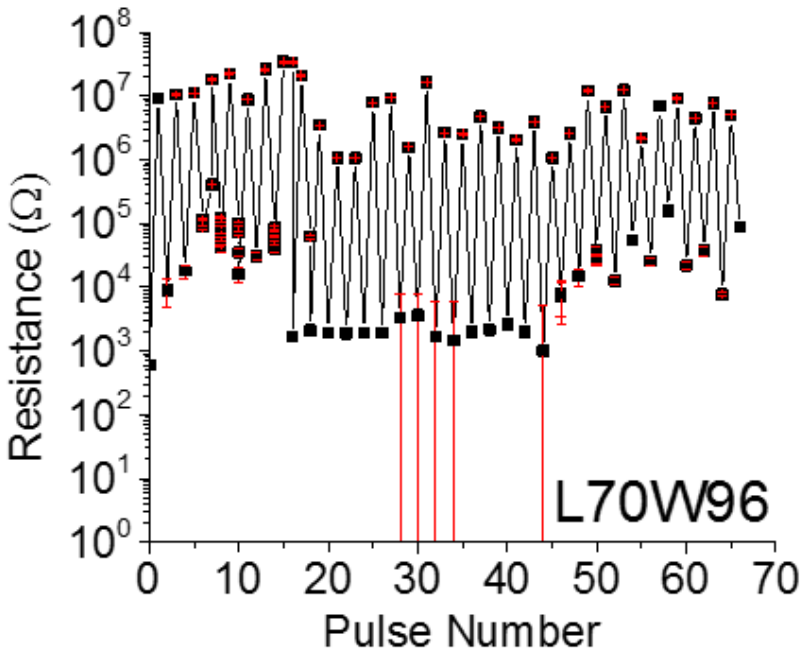


Figure 14: An origin plot of SET and RESET resistances during each cycle for the device PCMUCONK46_64215_1 L70W96.

Next, another device was chosen to be cycled to test the effect that cycling a device had on the resistance drift if left in a crystalline state. The device was cycled ten times and then left in a semi-crystalline state. Instead of varying the pulse amplitude during these cycles, the Reset pulse was kept at 2.85 V and the set pulse was kept at an amplitude of 2 V. The wavefrom was only sent once to set the device and once to reset the device. After only four cycles, the device reset-set window dropped dramatically and began to toggle bettwen a resistance of 10^4 and 10^5 Ω.

These resistance values do not fall in either a fully amorphous or fully crystalline state, and instead are in a "mixed" state. For these experiments, a mixed state was defined as a device with a resistance between 200 kΩ and 1 MΩ.

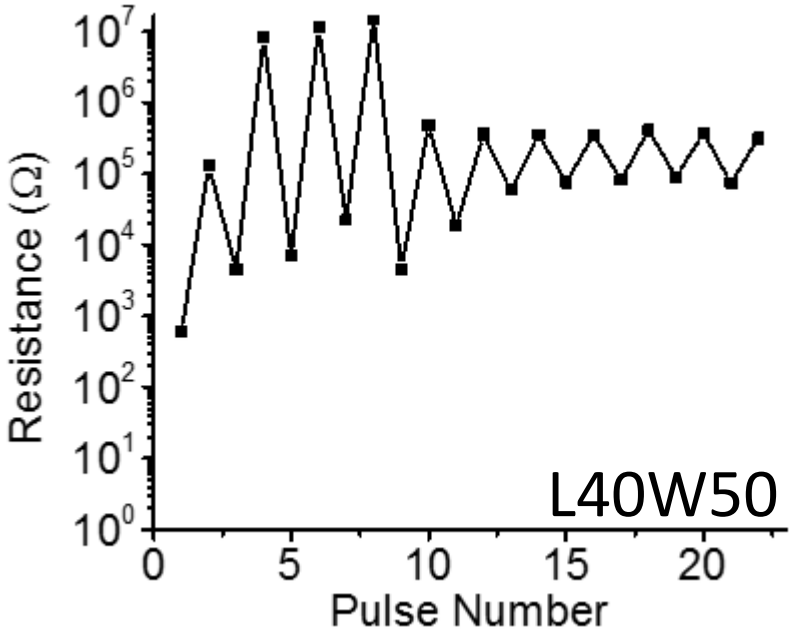


Figure 15: An origin plot of SET and RESET resistances during 10 cycles for the device L40W50.

Another device was chosen for its similar dimensions and initial crystalline resistance. It was used as the control and only cycled once with the same set and reset waveform. Both devices had a final mixed state resistance of around 320 kΩ. It was predicted that both of the devices would return to an FCC crystalline state at room temperature (300K). The drift of the two devices were monitored over time and plot in Figures 16 and 17.

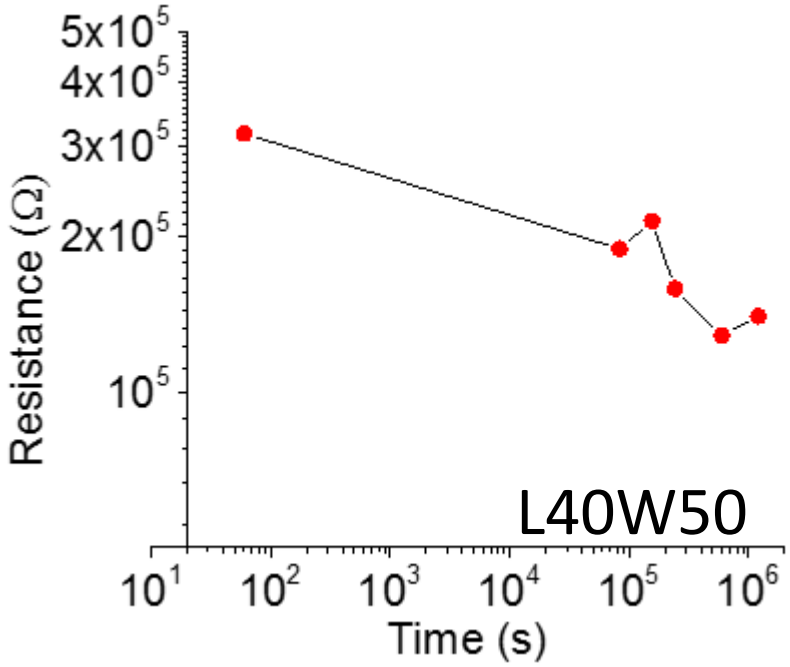


Figure 16: A plot of the drift of the resistnace for a device left in a crystalline state after being cycled 10 times.

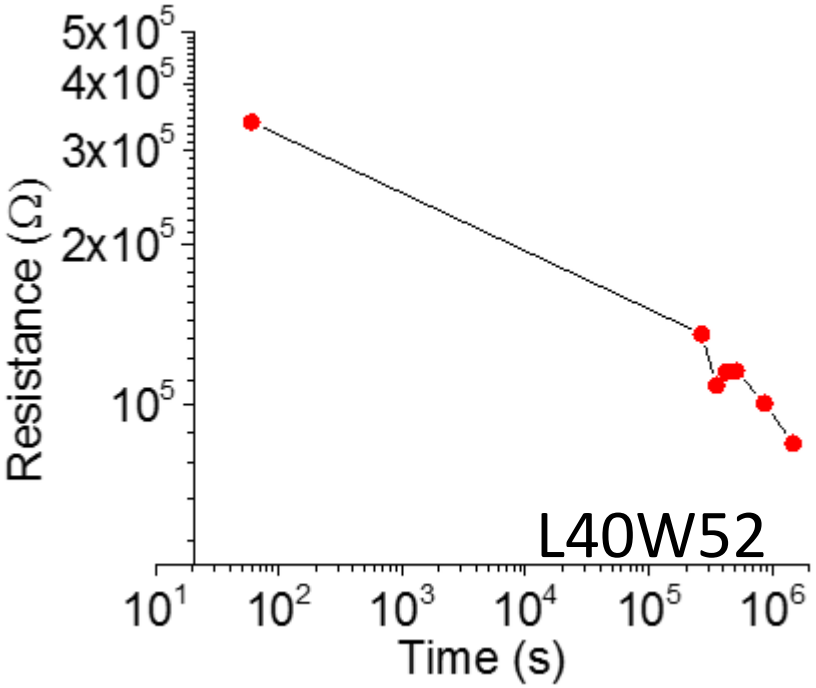


Figure 17: A plot of the drift of the resistnace for a device left in a crystalline state after being cycled once.

The resistance of both devices declined overtime. The device that was only cycled once rapidly decreased its resistance in the first few days and continued to become more conductive throughout the measurements. The device that was cycled 10 times also showed an initial decrease in resistance, but more quickly stabilized and remained at a higher crystalline resistance.

1MΩ AC Termination

The development of multi-bit-per-cell storage requires an understanding of the electrical configuration of the circuit that encompasses the GST. The components of the electrical circuit may have a dependence on the phase or resistance of the GST, or the metal contacts. For this reason, when an interesting RC charging and discharging occurred during a set of measurements, the reasons behind it were further investigated.

When conducting AC measurements with the PCM devices, the termination resistance is switched from 1 MΩ to 50 Ω to reduce the time constant in the internal circuit. During one set of measurements, on amorphized GST wires, the termination resistance was accidently set to 1 MΩ, and an unexpected phenomenon occurred. As the signal stepped up and stepped down, a charging and discharging effect occurred that the lab later named the "Mustache Effect." To better explain this phenomenon, a structured set of measurements were performed.

There were two different wire conditions that were tested at 300K under vacuum. The first condition consisted of pre-amorphized wires. Wires within the lengths 120-300nm and widths 80-420nm were amorphized and allowed to drift since the AC waveform did not immediately

follow the pulse. The wires had an initial amorphous resistance between 15MΩ-200MΩ. Next, long crystalline wires having the length of magnitude 10^{-6} m, were tested. These long wires were also FCC, but had a higher crystalline resistance comparable to the amorphized wires, 6MΩ-20MΩ. This was done to see if the effect had to do with amorphization of the cells or only correlated with a high resistance value.

It was discovered that when a positive offset is added to the applied voltage there is a positive charge and discharge, and when a negative offset added to the applied voltage there is a negative, or inverse, charge and discharge. Additionally, as the amplitude of the applied offset is increased, the peak current of the charging and discharging also increases. The opposite is true when a negative offset is applied. The results for the long crystalline, amorphous, and simulated results are show below in Figures 18, 19, and 20 respectively.

Long Crystalline

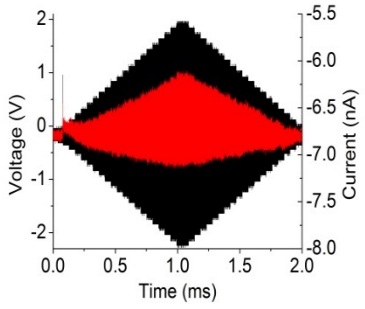
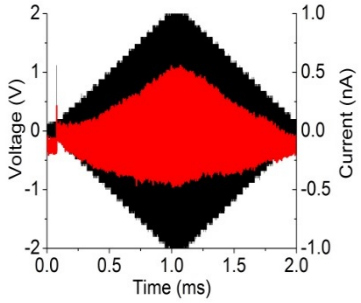
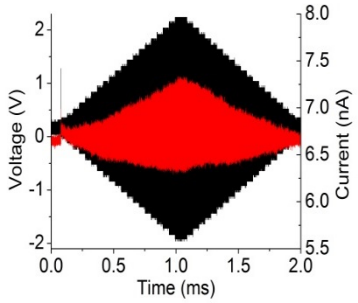
-800 mV offset	0mV offset	800 mV offset
		

Figure 18: Long crystalline wire with 21 MΩ resistance and -800 mV, 0 mV, and 800 mV applied offset.

Amorphous

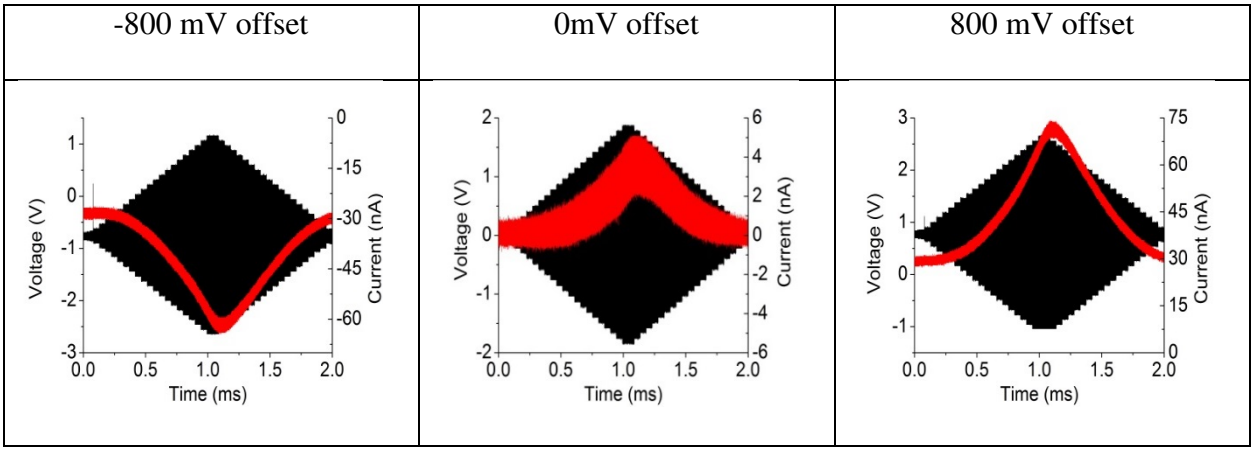


Figure 19: Amorphous wire L300 W200 with 32 MΩ resistance and -800mV, 0mV, and 800mV applied offset.

Simulated

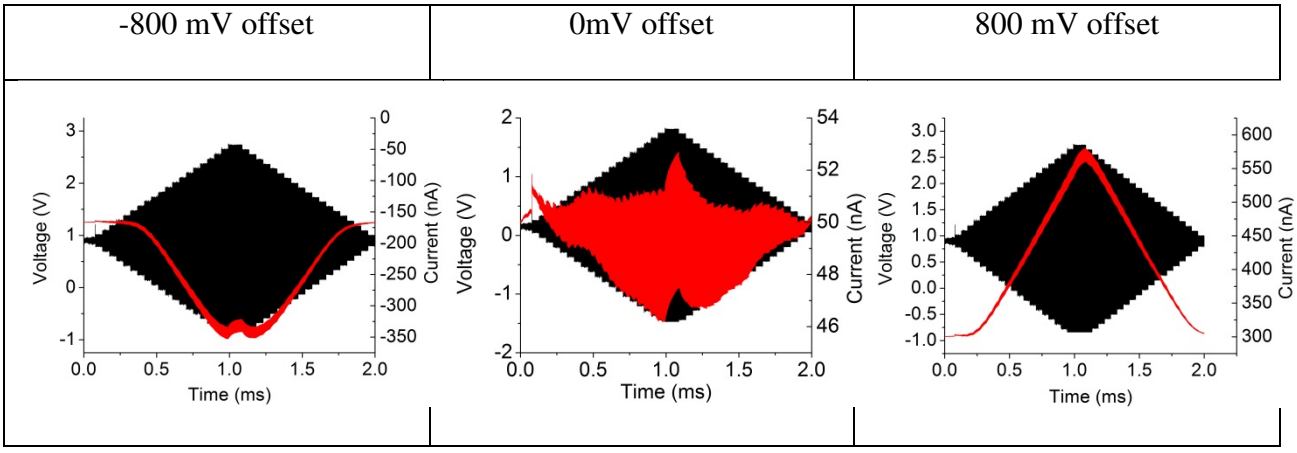


Figure 20: Simulated amorphous wire with 1 MΩ resistance and -800mV, 0mV, and 800mV applied offset.

One explanation to this charging is that there are two diodes being formed through the metal contacts and the GST wire. This is supported by the fact that in some of the I-V measurements, a nonlinear behavior was observed both before and after amorphization of the wire. Diodes have nonlinear I-V characteristics, and combined with the capacitors in the circuit, could cause the

charging and discharging seen. Schottky diodes can be formed through a contact between a semiconductor and a metal.[6] Since GST is a semiconductor, one of these diodes could be forming at each end of the wire contacts if the wire has been amorphized from metal to metal.

A model was created in LTspice to simulate the behaviors of the circuit using the knowledge of the components that are confirmed to be there. With these elements, measurements were simulated comparable to what was experimentally found. The largest inconstancy with this model is the GST wire resistance necessary to simulate similar results. The amorphized wires that were used to test for the charging effect had resistances between 35 MΩ and 50 MΩ, and the charging effect only appears in the simulation when the resistance of the wire is set to 1 MΩ or less.

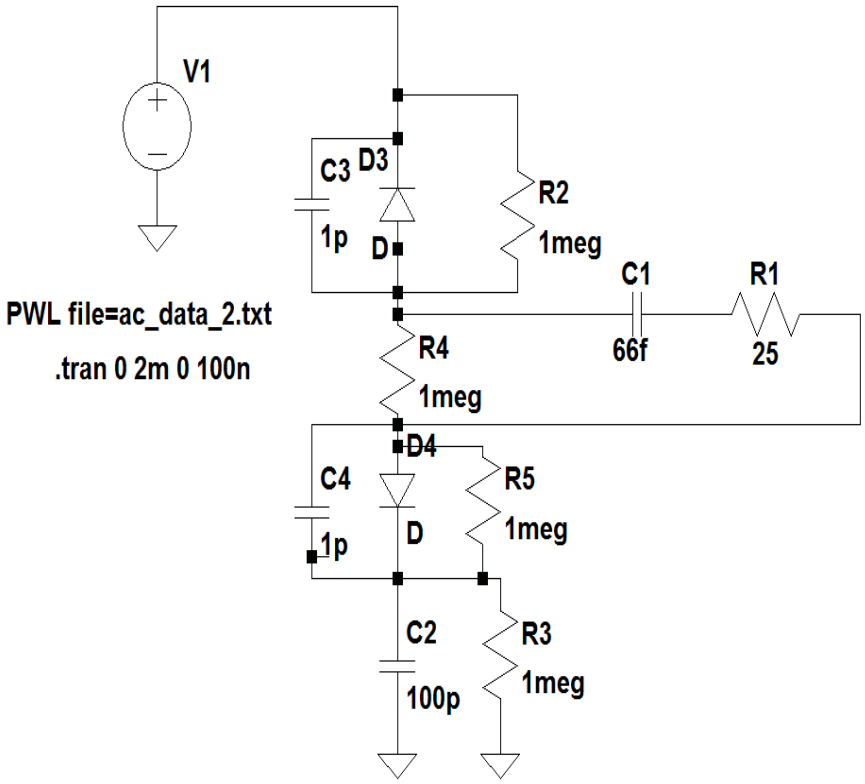


Figure 21: LTSpice simulation of the circuit incuding the opposite facing Schottky diodes.

An identical AC signal to the one used to measure the GST wire with the function generator was used in the simulation to reduce any extraneous variables. With the help of Nicholas Williams the AC signal was uploaded into LTSpice.

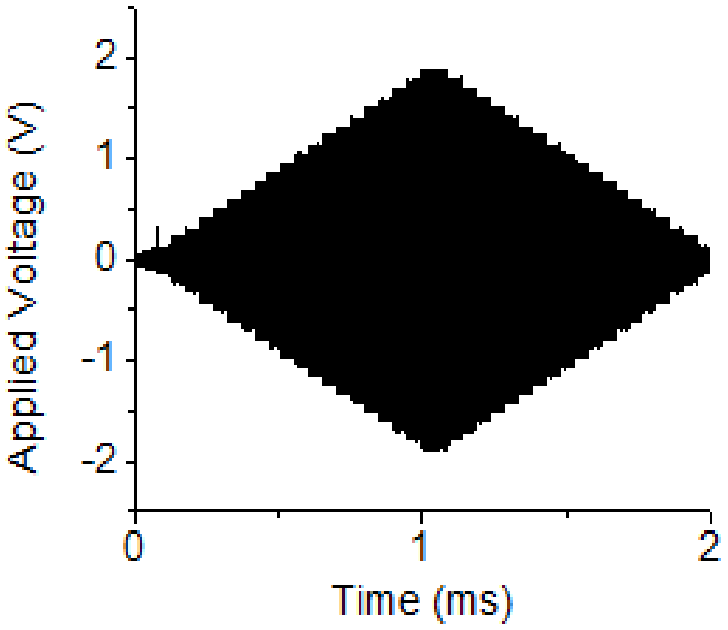


Figure 22: An Origin plot of the AC signal sent to amorphize and measure the wire.

The simulation results show similar characteristics to the experimental results, but the amount of current through the termination resistor is higher than the experimental measurements (as shown in Figure 23).

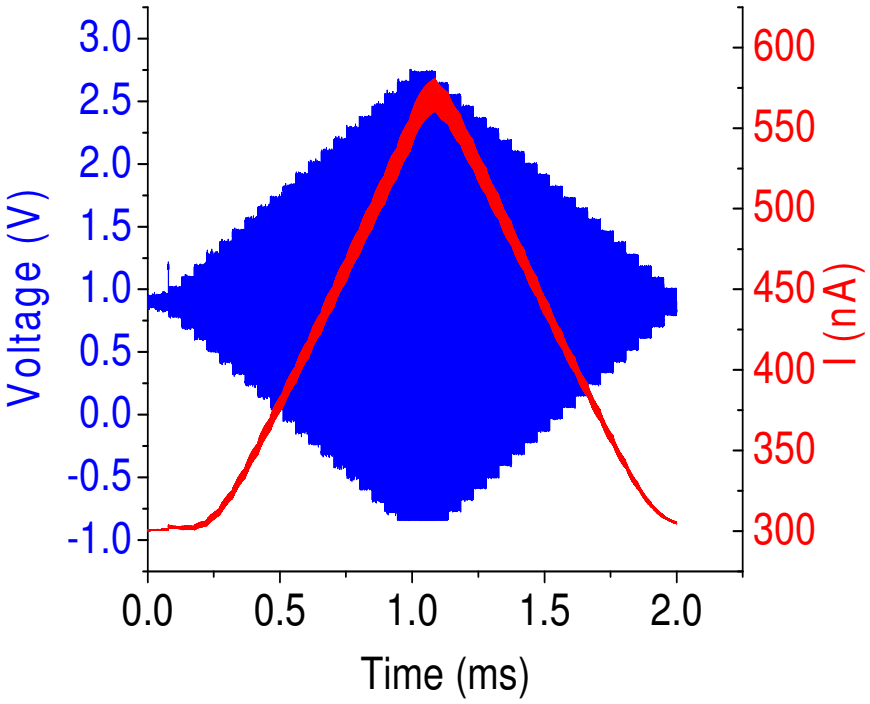


Figure 23: A graph of the simulation current though the termination resistor with a 700 mV bias..

When a postive bias is placed on the simulation voltage, the results of the measured current correspond to the shape of the experimental data. Based off of the experimental results, with an offset of 700 mV, the peak current in the simulation is predicted to be somewhere around 75 nA. Instead, the simulation produced a peak current around 580 nA. Similarly, when a negative bias was placed in the virtual circuit, the current was around 5 times the expected simulated current. The simulation diodes were preprogrammed from the LTspice library, and they are most likely too strong to represent the actual diode created in the GST contacts. This would cause the simulation current to be higher than the experimental current.

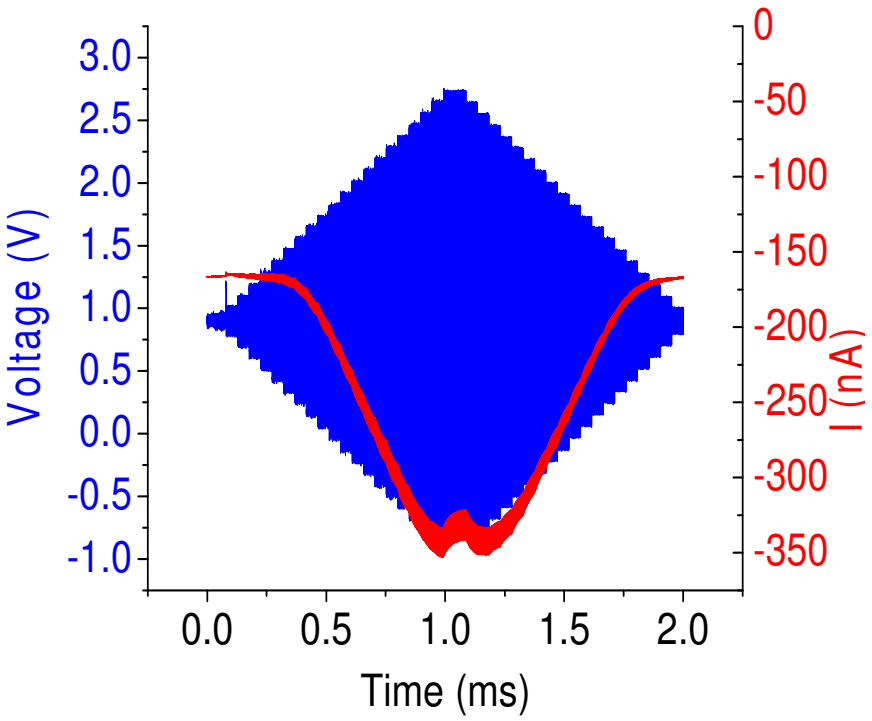


Figure 24: A plot of the simulation current through the termination resistor with a -700 mV bias.

When a negative bias is placed on the simulation voltage, there is a slight dip at the current peak that does not occur in the experimental measurements. This may be the resulting from the type of diodes that were used for the simulation.

Conclusion

The devices used in this experiment can be successfully toggled between the amorphous and crystalline state with a large enough gap to retain memory. This is only true when the Set and Reset pulse amplitudes are altered based off of the characteristics of the device during each cycle and not sent continuously. Sending a continuous cycling waveform produces 4-10 cycles with a large enough resistance gap for a good electrical reading, but as the device continues to cycle, the

gap decreases. Cycling a device multiple times may disturb the wires so that the stable crystalline resistance is higher than that of the devices which are only set once (or not cycled at all).

The Mustache Effect is most likely due to the result of Schottky diodes forming within the GST or between amorphous GST and the metal contacts. These opposite facing diodes that appear with the use of a 1MΩ termination resistance lead to large changing and discharging effects. A new model of the experimental circuit was designed based off of these observations. This RC nonlinearity has not been seen in pervious experiments and could play a vital role in designing the set-up for future experimentations.

References

[1] Wong, H-S. Philip, Simone Raoux, SangBum Kim, Jiale Liang, John P. Reifenberg, Bipin Rajendran, Mehdi Asheghi, and Kenneth E. Goodson. "Phase change memory." *Proceedings of the IEEE* 98, no. 12 (2010): 2201-2227.

[2] Qureshi, Moinuddin K., John Karidis, Michele Franceschini, Vijayalakshmi Srinivasan, Luis Lastras, and Bulent Abali. "Enhancing lifetime and security of PCM-based main memory with start-gap wear leveling." In *Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture*, pp. 14-23. ACM, 2009.

[3] Oosthoek, J. L. M., K. Attenborough, G. A. M. Hurkx, F. J. Jedema, D. J. Gravesteijn, and B. J. Kooi. "Evolution of cell resistance, threshold voltage and crystallization temperature during cycling of line-cell phase-change random access memory." *Journal of Applied Physics* 110, no. 2 (2011): 024505.

[4] Dirisaglik, Faruk, "High-Temperature Electrical Characterization of $Ge_2Sb_2Te_5$ Phase Change Memory Devices" (2014). *Doctoral Dissertations.* Paper 577. http://digitalcommons.uconn.edu/dissertations/577

[5] Burr, Geoffrey W., Pierre Tchoulfian, Teya Topuria, Clemens Nyffeler, Kumar Virwani, Alvaro Padilla, Robert M. Shelby, Mona Eskandari, Bryan Jackson, and Bong-Sub Lee. "Observation and modeling of polycrystalline grain formation in Ge2Sb2Te5." *Journal of Applied Physics* 111, no. 10 (2012): 104308.

[6] Mönch, Winfried. "Metal-semiconductor contacts: electronic properties."*Surface science* 299 (1994): 928-944.